IN THE CLAIMS

Please amend the claims as follows:

Claims 1-13 (Canceled).

Claim 14 (Currently Amended): A display device having an active matrix, comprising:

a plurality of scanners for selection lines;

a plurality of scanners for columns; and

B27 cont

a supplementary conductive column crossing over the selection lines and capacitively coupled to each of ~~them~~ the selection lines in such a way that each corresponding coupling capacitance has a value close to [[the]] a sum of ~~the~~ coupling capacitances formed between a given selection line and ~~the~~ columns which said given selection line crosses.

Claim 15 (Currently Amended): A display device according to ~~Claim~~ claim 14, wherein associated with said supplementary conductive column is a supplementary conductive line capacitively coupled with ~~it~~ the supplementary conductive column and associated with ~~it~~ the supplementary conductive column via a comparator circuit, said supplementary conductive line being coupled capacitively to each of the columns.

Claim 16 (Currently Amended): A display device according to claim 14 further comprising[[,]]:

a shift register coupled to said selection lines, said shift register ~~containing~~ comprising a plurality of cascaded stages, a given stage being responsive to two clock signals, said given stage having an output and an input, said input being coupled to an output of a preceding stage and to an output of a next stage, said given stage including[[,]] a first semiconductor

output device ~~switching~~ configured to switch the output of said given stage between high and low values of a first clock signal, the first semiconductor device being controlled by a potential of a first node connected:

to the output of the preceding stage via a second semiconductor device controlled by the output of the preceding stage,

to a negative potential via a third semiconductor device controlled by the output of the next stage,

to a second clock signal via a first capacitance, and

to the output of the given stage via a second capacitance.

B27

Claim 17 (New): A display device according to claim 14 further comprising:

a shift register coupled to said selection lines, said shift register comprising a plurality of cascaded stages, a given stage being responsive to two clock signals, said given stage having an output and an input, said input being coupled to an output of a preceding stage and to an output of a next stage, said given stage including a first semiconductor output device configured to switch the output of said given stage between high and low values of a first clock signal, the first semiconductor device being controlled by a potential of a first node connected:

to the output of the preceding stage via a second semiconductor device controlled by the output of the preceding stage,

to a second clock signal via a first capacitance,

to the output of said given stage via a second capacitance, said given stage output being connected to ground via a third semiconductor device controlled by a second node, and

to ground across a fourth semiconductor device controlled by the second node, the second node being further connected:

to the output of the preceding stage via a fourth capacitance,

to ground via a fifth semiconductor device controlled by the output of the preceding stage,

to the output of the next stage via first and second clamping transistors mounted in parallel and controlled, one by the second node and the other by the output of the next stage, and

to a terminal of the third semiconductor device connected to ground by a fifth capacitance.

Claim 18 (New): A display device according to claim 14 further comprising:

a shift register coupled to said selection lines, said shift register comprising a plurality of cascaded stages, a given stage being responsive to two clock signals, said given stage having an output and an input, said input being coupled to an output of a preceding stage and to an output of one of a next stage and of a stage following the next stage, said given stage including a first semiconductor output device switching the output of said given stage between high and low values of a first clock signal, the first semiconductor device being controlled by a potential of a first node connected:

to the output of the preceding stage via a second semiconductor device controlled by the output of the preceding stage,

to a second clock signal via a first capacitance,

to the output of the given stage via a second capacitance, the given stage output being connected to ground via a fourth semiconductor device controlled by a second node, and

to a negative potential via a third semiconductor device controlled by the second node which is further connected to one of the output of the next stage and of the stage following the next stage.

Claim 19 (New): A display device according to claim 14 further comprising:

a shift register coupled to said selection lines, said shift register comprising a plurality of cascaded stages, a given stage being responsive to two clock signals, said given stage having an output and an input, said input being coupled to an output of a preceding stage and to an output of a next stage, said given stage including a first semiconductor output device switching the output of said given stage between high and low values of a first clock signal, the first semiconductor device being controlled by a potential of a first node connected:

to the output of the preceding stage via a second semiconductor device controlled by the output of the preceding stage,

to a signal via a third semiconductor device controlled by the output of the next stage,

to a second clock signal via a first capacitance, and

to the output of the given stage via a second capacitance, the stage output being connected to ground via a fourth semiconductor device controlled by a zero-reset signal.

B27

Claim 20 (New): A display device according to claim 14 further comprising:

a shift register coupled to said selection lines, said shift register comprising a plurality of cascaded stages, a given stage being responsive to two clock signals, said given stage having an output and an input, said input being coupled to an output of a preceding stage and to an output of a next stage, said given stage including a first semiconductor output device switching the output of said given stage between high and low values of a first clock signal, the first semiconductor device being controlled by a potential of a first node connected:

to the output of the preceding stage via a second semiconductor device controlled by the output of the preceding stage,

to a constant negative potential via a third semiconductor device controlled by one of three clock signals,

B3 Cont'd

to a second clock signal via a first capacitance, and

to the output of the given stage via a second capacitance, the stage output being connected to ground via a fourth semiconductor device controlled by a zero-reset signal.